CLAIMS

What is claimed is:

1. A semiconductor structure comprising:
   (a) a substrate including at least one post, the post size and spacing having a nanoscale width of approximately 100 nanometers or less; and
   (b) a laterally grown portion extending laterally from the post over the substrate.
2. The structure according to claim 1 wherein the post is formed by sub-micron lithography.
3. The structure according to claim 2 wherein the post is formed by edge definition lithography.
4. The structure according to claim 1 wherein the laterally grown portion is spaced vertically from the substrate.
5. The structure according to claim 1 wherein the post has a width of approximately 30 nanometers or less.
6. The structure according to claim 1 wherein the laterally grown portion comprises outermost pointed fronts.
7. The structure according to claim 1 wherein the laterally grown portion comprises outermost flat fronts.
8. The structure according to claim 1 wherein the laterally grown portion comprises an at least generally triangular shape.
9. A semiconductor structure comprising:
   (a) a substrate having dislocation defects spaced apart by an average distance characteristic for the substrate;
   (b) at least one post included on the substrate, the post having a width less than the average distance separating the dislocation defects characteristic for the substrate; and
   (c) a laterally grown portion extending laterally from the post and over the substrate.

10. The structure according to claim 9 wherein the post is formed by sub-micron lithography.

11. The structure according to claim 10 wherein the post is formed by edge definition lithography.

12. The structure according to claim 9 wherein the laterally grown portion is spaced vertically from the substrate.

13. The structure according to claim 9 wherein the post has a width of approximately 30 nanometers or less.

14. The structure according to claim 9 wherein the laterally grown portion comprises outermost pointed fronts.

15. The structure according to claim 9 wherein the laterally grown portion comprises outermost flat fronts.

16. The structure according to claim 9 wherein the laterally grown portion comprises an at least generally triangular shape.

17. A semiconductor structure comprising:

(a) a substrate including a plurality of posts, each post having a nanoscale pitch of approximately 100 nanometers or less; and

(b) each post having a laterally grown portion extending laterally over the substrate, wherein a spacing distance separating the laterally grown portions of the posts is approximately 50 nanometers or less.

18. The structure according to claim 17 wherein the post is formed by sub-micron lithography.

19. The structure according to claim 18 wherein the post is formed by edge definition lithography.

20. The structure according to claim 17 wherein the posts are separated by a spacing distance of approximately 5 nanometers or less.

21. The structure according to claim 17 wherein the posts have a pitch of approximately 30 nanometers or less.

22. The structure according to claim 17 wherein each laterally grown portion comprises outermost pointed fronts.

23. The structure according to claim 17 wherein each laterally grown portion comprises outermost flat fronts.

24. The structure according to claim 17 wherein each laterally grown portion comprises an at least generally triangular shape.

25. The structure according to claim 17 comprising a molecular electronics device attached between the laterally grown portions of the posts.

26. The structure according to claim 17 wherein the laterally grown portions are coalesced to form a layer.

27. The structure according to claim 19 wherein the coalesced layer has reduced dislocation defects.

28. The structure according to claim 17 wherein the posts comprise a plurality of three-dimensional interconnect nodes.

29. The structure according to claim 28 further comprising a molecular electronic device attached between at least two of the interconnect nodes.

30. A semiconductor structure comprising:

(a) a substrate having a dislocation defects spaced apart by an average distance characteristic for the substrate;

(b) a plurality of posts included on the substrate; and

(c) a laterally grown portion extending laterally from each post and over the substrate, wherein a spacing between adjacent laterally growth portions from adjacent posts is less than the average distance separating the dislocation defects characteristic for the substrate.

31. The structure according to claim 30 wherein the post is formed by sub-micron lithography.

32. The structure according to claim 31 wherein the post is formed by edge definition lithography.

33. The structure according to claim 30 wherein the laterally grown portion is spaced vertically from the substrate.

34. The structure according to claim 30 wherein the post has a width of approximately 30 nanometers or less.

35. The structure according to claim 30 wherein the laterally grown portion comprises outermost pointed fronts.

36. The structure according to claim 30 wherein the laterally grown portion comprises outermost flat fronts.

37. The structure according to claim 30 wherein the laterally grown portion comprises an at least generally triangular shape.

38. A semiconductor structure comprising:

(a) a substrate including a plurality of posts, each post having a nanoscale pitch of approximately 100 nanometers or less; and

(b) each post having a laterally grown portion extending laterally over the substrate, wherein the laterally grown portions extend and coalesce to form a coalesced layer.

39. The structure according to claim 30 wherein each post is formed by sub-micron lithography.

40. The structure according to claim 31 wherein the post is formed by edge definition lithography.

41. The structure according to claim 30 wherein the coalesced layer has reduced dislocation defects.

42. A method for forming a laterally grown semiconductor structure comprising:

(a) forming at least one post on a substrate, the post having a nanoscale width of approximately 100 nanometers or less; and

(b) growing a laterally grown portion from the post extending laterally from the post over the substrate.

43. The method according to claim 42 comprising growing the post by sub-micron lithography.

44. The method according to claim 43 comprising growing the post by edge definition lithography.

45. The method according to claim 43 comprising growing the laterally grown portion to be spaced vertically from the substrate.

46. The method according to claim 42 wherein the post has a width of approximately 100 nanometers or less.

47. The method according to claim 42 comprising growing the laterally grown portion wherein the laterally grown portion comprises outermost pointed fronts.

48. The method according to claim 42 comprising growing the laterally grown portion structure wherein the laterally grown portion comprises outermost flat fronts.

49. The method according to claim 42 comprising growing the laterally grown portion structure wherein the laterally grown portion comprises an at least generally triangular shape.

50. A method for forming a laterally grown semiconductor structure comprising:

(a) providing a substrate having dislocation defects spaced apart by an average distance characteristic for the substrate;

(b) forming at least one post on the substrate, the post having a width less than the average distance separating the dislocation defects characteristic for the substrate; and

(c) growing a laterally grown portion from the post extending laterally from the post and over the substrate.

51. The method according to claim 50 comprising growing the post by sub-micron lithography.

52. The method according to claim 50 comprising growing the post by edge definition lithography.

53. The method according to claim 50 comprising growing the laterally grown portion to be spaced vertically from the substrate.

54. The method according to claim 50 wherein the post has a width of approximately 100 nanometers or less.

55. The method according to claim 50 comprising growing the laterally grown portion wherein the laterally grown portion comprises outermost pointed fronts.

56. The method according to claim 50 comprising growing the laterally grown portion structure wherein the laterally grown portion comprises outermost flat fronts.

57. The method according to claim 50 comprising growing the laterally grown portion structure wherein the laterally grown portion comprises an at least generally triangular shape.

58. A method for forming a laterally grown semiconductor structure comprising:

(a) forming a plurality of posts on a substrate, each post having a nanoscale width of approximately 100 nanometers or less; and

(b) growing a laterally grown portion from each of the posts extending laterally over the substrate, wherein a spacing distance separating the laterally grown portions of the posts is approximately 50 nanometers or less.

59. The method according to claim 58 wherein each post is formed by sub-micron lithography.

60. The method according to claim 59 wherein each post is formed by edge definition lithography.

61. The method according to claim 58 comprising growing each laterally grown portion to be spaced vertically from the substrate.

62. The method according to claim 58 wherein each post has a width of approximately 100 nanometers or less.

63. The method according to claim 58 comprising growing each laterally grown portion wherein the laterally grown portion comprises outermost pointed fronts.

64. The method according to claim 58 comprising growing each laterally grown portion structure wherein the laterally grown portion comprises outermost flat fronts.

65. The method according to claim 58 comprising growing each laterally grown portion structure wherein the laterally grown portion comprises an at least generally triangular shape.

66. The method according to claim 58 comprising attaching a molecular electronic device to and between adjacent laterally grown portions of adjacent posts.

67. The method according to claim 58 comprising forming a plurality of three dimensional interconnect nodes for molecular device attachment from the laterally grown posts.

68. The method according to claim 67 comprising attaching a molecular electronic device to and between adjacent laterally grown portions of adjacent posts.

69. A method of controlling electron affinity in a laterally overgrown semiconductor structure, comprising:

(a) providing a substrate with a plurality of posts included on the substrate, each post having laterally overgrown portions and wherein the laterally overgrown portions of adjacent posts are spaced apart a nanoscale dimension;

(b) interconnecting a molecular electronic device between and to the laterally overgrown portions of adjacent posts; and

(c) controlling composition of the laterally overgrown portions to control electron affinity between the laterally overgrown portions and the molecular electronics device.